REMARKS

Claims 1-69 are pending in the application with claims 1, 4, 7, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62 and 66 being independent. Claims 1, 4, 7, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62 and 66 have been amended.

Interview

Initially, applicant would like to thank the Examiner for the interview granted to the undersigned attorney on September 16, 2003, at which the proposed amendments to the drawings were discussed. As noted at the interview, this application was inadvertently filed with a set of drawings corresponding to a related application. The drawings have been amended to address this error per the discussions at the interview. As also discussed, a detailed written explanation of how the drawing amendments are supported by the specification is provided.

Drawing Amendments

Figs. 2, 4A, 4B, 7, 8, 9B-16, 27 and 30A-30C have been amended as described below. The amendments are supported by the specification. No new matter has been added.

Fig. 2

As illustrated in the annotated sheet, the following changes have been made to Fig. 2:

(1) Tr3 and Tr4 have been relabeled as Tr4 and Tr5, respectively. This change is supported by the application at page 8, lines 23-29, which states that gate electrodes of Tr4 and Tr5 are connected to scanning line Gj, and that a source or drain region of Tr4 is connected to a drain region of Tr1.

(2) Tr3 has been provided between Tr2 and OLED 104, with the gate electrode of Tr3 being connected to the source or drain region of Tr5. This change is supported by the specification. At page 8, lines 17-22, the specification states that pixel 101 has at least Tr1, Tr2, Tr3, Tr4, and Tr5. From this description, it is apparent that Fig. 2 is meant to include a circuit having at least five thin film transistors. At page 8, lines 27-29 and page 9, lines 4-6, the

specification states that a source or drain region of Tr5 is connected to a gate electrode of Tr3, a drain region of Tr2 is connected to a source region of Tr3, and a drain region of Tr3 is connected to a pixel electrode of OLED 104.

(3) The drain region of Tr2 is connected to a gate electrode of Tr2, and the drain region of Tr2 is connected to the source region of Tr3. The description at page 8, lines 30 to page 9, line 3, states that a gate electrode of Tr2 should be connected to a drain region of Tr2, and that the drain region of Tr2 should be connected to a source region of Tr3.

(4) The storage capacitor 105 is formed between the gate electrode of Tr3 and the power supply line Vi. At page 9, lines 23-24, the specification states that the storage capacitor 105 is formed between a gate electrode of Tr3 and a power supply line Vi.

Figs. 4A and 4B

Figs. 4A and 4B illustrate operation of the circuit of Fig. 2, and have been amended to be consistent with the amendments to Fig. 2 and the accompanying text. The amendments to Figs. 4A and 4B are appropriate for the same reasons that the amendments to Fig. 2 are appropriate.

Fig. 7

The amendments to Fig. 7 are very similar to the amendments to Fig. 2. As illustrated in the annotated sheet, the following changes have been made to Fig. 7:

(1) Tr3 and Tr4 have been replaced with Tr4 and Tr5, respectively. At page 15, lines 1-5, the specification states that the gate electrodes of Tr4 and Tr5 are connected to a scanning line Gj, and that a source or drain region of Tr4 is connected to a drain region of Tr1.

(2) Tr3 has been provided between Tr2 and OLED 104, with the gate electrode of Tr3 connected to a source or drain region of Tr5. At page 14, lines 25-30, the specification states that pixel 101 has at least Tr1, Tr2, Tr3, Tr4, and Tr5, which establishes that a fifth transistor needs to be included. At page 15, lines 5-7 and lines 11-15, the specification states that a source or drain region of Tr5 is connected to a gate electrode of Tr3, a drain region of Tr2 is connected

to a source region of Tr3, and a drain region of Tr3 is connected to a pixel electrode of OLED 104.

(3) The drain region of Tr2 is connected to the gate electrode of Tr2, and the drain region of Tr2 is connected to the source region of Tr3. See page 15, lines 11-12.

(4) The storage capacitor 105 is formed between the gate electrode of Tr3 and the power supply line Vi. See page 15, lines 27-28.

Fig. 8

The amendments to Fig. 8 are very similar to the amendments to Figs. 2 and 7. As illustrated in the annotated sheet, the following changes have been made to Fig. 8:

(1) Tr3 and Tr4 have been replaced with Tr4 and Tr5, respectively. At page 17, lines 22-26, the specification states that gate electrodes of Tr4 and Tr5 are connected to a scanning line Gj, and that a source or drain region of Tr4 is connected to a drain region of Tr1.

(2) Tr3 is provided between Tr2 and OLED 104, and a gate electrode of Tr3 is connected to a source or drain region of Tr5. See page 16, lines 16-21 and 26-28, and page 17, lines 3-5.

(3) A drain region of Tr2 is connected to a gate electrode of Tr2, and the drain region of Tr2 is connected to a source region of Tr3. See page 17, lines 2-3.

(4) A storage capacitor is formed between a gate electrode of Tr3 and a power supply line Vi. See page 17, lines 18-19.

Figs. 9B-13

Figs. 9A-13 illustrate a method of manufacturing a light emitting device. The method includes simultaneously forming, on a same substrate, transistors Tr2, Tr3 and Tr5 of a pixel portion and transistors of a driving portion, and is described in detail at page 18, line 5 to page 29, line 30. As discussed at the interview, applicant does not believe that these figures are necessary to enable the claimed subject matter, but is amending them in the interest of clarity.

From Fig. 11B, it is noted that a left portion from a doted line in each Figs. 9A-11B is a pixel portion, and it is expected that transistors Tr2, Tr3, and Tr5 are provided in the left portion.

As such, Figs. 9B-11B have been amended to show that two transistors Tr2 and Tr3 are formed on a same semiconductor layer. Support for this change is provided in amended Figs. 2, 7, and 8, and the accompanying text, which show that transistors Tr2 and Tr3 are formed in series: in amended Figs. 15 and 16, and the accompanying text, which show that the transistors Tr2 and Tr3 are formed on the same semiconductor layer; and in amended Figs. 2, 7, 8, 15 and 16, which also show that Tr3 is connected to a pixel electrode. In view of this, Figs. 9B-11B have been amended to show two transistors Tr2 and Tr3 formed on a semiconductor layer 905, with Tr3 connected to a pixel electrode 948. In addition, it is clear that Tr5 is formed on a semiconductor layer 904.

As an additional note, amended Fig. 10B shows that an impurity element for imparting p-type is added to Tr2 and Tr3. This is supported by the specification at page 23, lines 22-24 and page 9, lines 17-20.

Fig. 12 is a top view of a pixel after the process up through the step of Fig. 11A is finished. See page 26, lines 29-30. Since a sectional view taken along the line A-A' in Fig. 12 corresponds to the area indicated by A-A' in Fig. 11A (see page 27, lines 2-3), Tr4 has been amended as Tr5, and Tr3 has been provided between the pixel electrode 948 and Tr2 as shown in amended Fig. 12. In addition, Tr3 has been connected to the pixel electrode through a wiring line 946 as shown in the amended Fig. 12.

Fig. 12 has also been amended for consistency with Fig. 2. First, Tr3 has been replaced with Tr4. This amendment is supported by the specification at page 8, lines 23-29, which states that a gate electrode of Tr4 is connected to scanning line Gj and a source or drain region of Tr4 is connected to the drain region of Tr1. Next, as shown in Fig. 2, a gate electrode of Tr2 is connected to a drain region of Tr2, and the drain region of Tr2 is connected to a source region of Tr3. In view of this, a common impurity region of Tr2 and Tr3 is shown in Fig. 12 as being connected to the gate electrode of Tr2 through a connection wiring line 943. Next, as shown in Fig. 2, a gate electrode of Tr3 is connected to a source or drain region of Tr5. This is shown in Fig. 12, by connecting the gate electrode of Tr3 to the source or drain region of Tr5 through a connection wiring 945, which is also supported at the specification at page 8, lines 27-29.

Finally, as shown in the correct Fig. 2, a storage capacitor is formed between a gate electrode of Tr3 and a power supply line Vi, which is now shown in Fig. 12. This is also supported at page 9, lines 23-24. In addition, since Tr3 and the other transistors are simultaneously formed as taught in Fig. 9A-11B, the hatching of wirings associated with Tr3 is also supported by the original disclosure of the specification.

In view of the discussion at page 27, lines 4-5, Fig. 13 has been amended to replace Tr3 with Tr4.

Figs. 14A and 14B

Figs. 14A and 14B are being amended to be consistent with Figs. 11A and 11B. As discussed at the interview, applicant does not believe that these figures are necessary to enable the claimed subject matter, but is amending them in the interest of clarity. Support for the amendments may be found in the discussion of Figs. 11A and 11B above, and in the specification at page 30, lines 1-8, which states that the process through the formation of a second interlayer insulating film 939 is the same as in Embodiment 1.

Fig. 15

As noted in the specification at page 33, lines 13-14, Fig. 15 is a top view of the pixel as shown in Fig. 7. Accordingly, Fig. 15 has been amended to be consistent with Fig. 7. As discussed at the interview, applicant does not believe that Fig. 15 is necessary to enable the claimed subject matter, but is amending it in the interest of clarity.

Fig. 15 has been amended to correct Tr3 and Tr4 to be Tr4 and Tr5, respectively. This amendment is supported at page 33, lines 20-27.

Fig. 15 has also been amended to include Tr3 between Tr2 and the pixel electrode 223. A source region or a drain region of Tr3 is connected to pixel electrode 223 through connection wiring line 222. This amendment is supported at page 34, lines 5-7.

Fig. 15 has also been amended to have a drain region of Tr2 connected to a gate electrode of Tr2 and to a source region of Tr3 through a connection wiring line 221. This is supported at page 33, line 29, to page 34, line 1.

Fig. 15 has also been amended to show a storage capacitor formed between a gate electrode of Tr3 and a power supply line 217. This amendment is supported at page 34, lines 4-5 and lines 8-14.

All of the connections described above are shown in the amended Fig. 7. In addition, since Tr3 and the other transistors are simultaneously formed as discussed with respect to Figs. 9A-11B, the hatching of wirings associated with Tr3 is also supported by the original disclosure of the specification.

Fig. 16

As noted in the application at page 34, lines 26-27, Fig. 16 is a top view of the pixel as shown in Fig. 8. Accordingly, Fig. 16 has been amended to be consistent with Fig. 8. As discussed at the interview, applicant does not believe that Fig. 16 is necessary to enable the claimed subject matter, but is amending it in the interest of clarity.

Fig. 16 has been amended to correct Tr3 and Tr4 to be Tr4 and Tr5, respectively. This amendment is supported at page 35, lines 3-10.

Fig. 16 has also been amended to provide Tr3 between Tr2 and OLED 104. A source region or a drain region of Tr3 is connected to a pixel electrode 323 through a connection wiring line 322. This amendment is supported at page 35, lines 17-20.

Fig. 16 has also been amended to have a drain region of Tr2 connected to a gate electrode of Tr2 and a source region of Tr3 through a connection wiring line 321. This is also supported at page 33, lines 11-14.

Fig. 16 has also been amended to show a storage capacitor formed between the gate electrode of Tr3 and the power supply line 317. This correction is supported at page 34, lines 4-5 and lines 8-14.

All of the connections described above are shown in the amended Fig. 8. In addition, since Tr3 and the other transistors are simultaneously formed as discussed with respect to Figs. 9A-11B, the hatching of wirings associated with Tr3 is also supported by the original disclosure of the specification.

Fig. 27

Support for the changes to Fig. 27 may be found at page 36, lines 13-15. As discussed at the interview, applicant does not believe that Fig. 27 is necessary to enable the claimed subject matter, but is amending it in the interest of clarity.

Figs. 30A-30C

Each of Figs. 30A-30C has been amended (1) to replace Tr3 and Tr4 with Tr4 and Tr5, respectively; (2) to provide Tr3 between Tr2 and OLED 104, with a gate electrode of Tr3 connected to a source or drain region of Tr5; (3) to connect a drain region of Tr2 to a gate electrode of Tr2, and to connect the drain region of Tr2 to a source region of Tr3; (4) to form a storage capacitor between a gate electrode of Tr3 and a power supply line Vi; and (5) to provide Tr6.

At page 52, lines 24-29, the specification states that pixel 701 (Fig. 30A) has at least Tr1, Tr2, Tr3, Tr4, Tr5, and Tr6. The specification states that pixel 711 (Fig. 30B) and pixel 721 (Fig. 30C) has transistors with the same label at, respectively, page 54, lines 13-18, and page 56, lines 1-6. From these descriptions, it is understood that circuits having at least six thin film transistors are intended to be shown.

Support for replacing Tr3 and Tr4 with Tr4 and Tr5, respectively, may be found at page 52, line 30 to page 53, line 6 (for Fig 30A); page 54, lines 19-23 (for Fig. 30B); and page 56, lines 7-11 (for Fig. 30C), each of which states that gate electrodes of Tr4 and Tr5 are connected to a scanning line Gaj, and that a source or drain region of Tr4 is connected to a drain region of Tr1.

Support for providing Tr3 between Tr2 and OLED 104, with a gate electrode of Tr3 connected to a source or drain region of Tr5, may be found at page 53, lines 4-6, 11, and 16-17 (for Fig. 30A); page 54, lines 23-25 and 30, and page 55, lines 5-6 (for Fig. 30B); and page 56, lines 11-13, 17 and 23-24 (for Fig. 30C), each of which describes a source or drain region of Tr5 connected to a gate electrode of Tr3, a drain region of Tr2 connected to a source region of Tr3, and a drain region of Tr3 connected to a pixel electrode of an OLED.

Support for connecting a drain region of Tr2 to a gate electrode of Tr2, and a drain region of Tr2 to a source region of Tr3, may be found at page 53, lines 10-11 (for Fig. 30A); page 54, lines 29-30 (for Fig. 30B); and page 56, lines 17-18 (for Fig. 30C).

Support for forming a storage capacitor between a gate electrode of Tr3 and a power supply line Vi may be found at page 54, lines 1-2 (for Fig. 30A); page 55, lines 20-21 (for Fig. 30B); and page 57, lines 8-9 (for Fig. 30C).

Support for providing Tr6 may be found at page 53, lines 12-15 (for Fig. 30A); page 55, lines 1-4 (for Fig. 30B); and page 56, lines 19-22 (for Fig. 30C), each of which describes a gate electrode of Tr6 being connected to a second scanning line Gbj, a source or drain region of Tr6 being connected to a power supply line Vi, and the other being connected to a gate electrode of Tr1 and Tr2.

Objection to Specification

The title has been amended in response to the Examiner's suggestion, and minor amendments have been made to the specification to correct clerical errors. No new matter has been added.

The Examiner has objected to the specification. Initially, as to the Examiner's question regarding the distinction between embodiments and embodiment modes, applicant notes that an embodiment is an example of an embodiment mode. Thus, an embodiment is used to specify or explain an embodiment mode more concretely or with more particularity.

The amendments to the drawings are believed to address the remainder of the objections.

Objection to Drawings

The Examiner has objected to the drawings for failure to show transistor Tr5. This objection has been addressed by the amendments to the drawings.

Rejection Under Section 112, First Paragraph

These rejections appear to be based on a failure of the drawings to show certain claim elements, and to the use of "drain region thereof" in the independent claims. Each of the independent claims has been amended to replace "drain region thereof" with "drain region of the second transistor". These amendments, in combination with the amendments to the drawings, are believed to address these rejections.

Obviousness Rejection

Claims 1-69 have been rejected as being obvious over Sedra and Smith in view of Kawashima and Yumoto. Applicant requests reconsideration and withdrawal of this rejection because neither Sedra and Smith, Kawashima, Yumoto, nor any combination of the three, describes or suggests having a gate electrode of a first transistor connected to a gate electrode of a second transistor and to a drain region of the second transistor; a source region of a third transistor connected to a drain region of the second transistor, and a drain region of the third transistor connected to a pixel electrode of an organic light emitting diode; and a drain region of the first transistor and a gate electrode of the third transistor connected to each other for a certain period in one frame period, as recited in each of the independent claims.

Provisional Double Patenting Rejection

The claims have been provisionally rejected for obviousness-type double patenting as being unpatentable over claims 1-197 of Application No. 10/077,830 and claims 1-62 of Application No. 10/230,068. Applicant will consider whether to file a terminal disclaimer when the claims are otherwise found to be allowable.

Applicant submits that all claims are in condition for allowance.

Enclosed is a $950 for the Petition for Extension of Time fee. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: October 27, 2003

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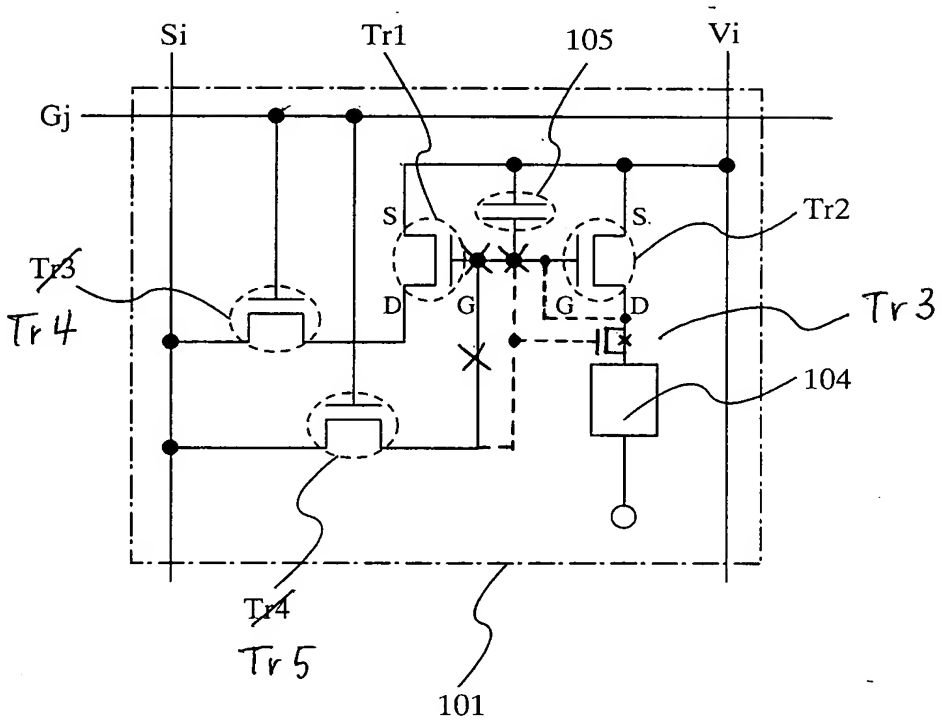

Fig. 2

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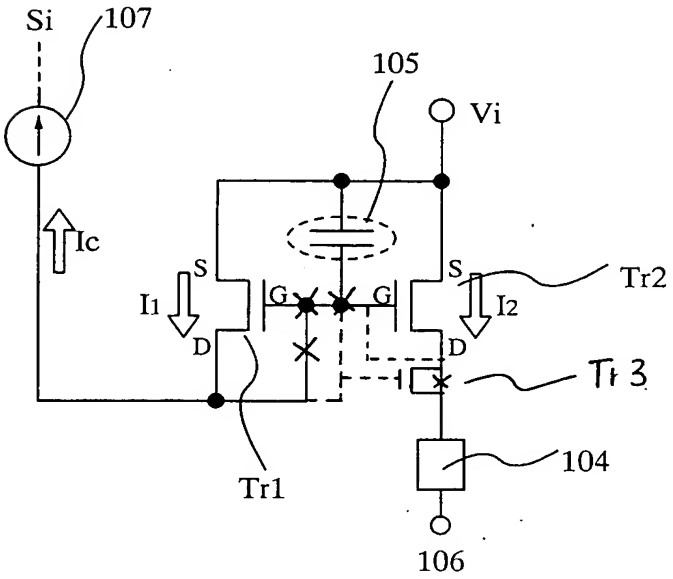

Fig. 4A

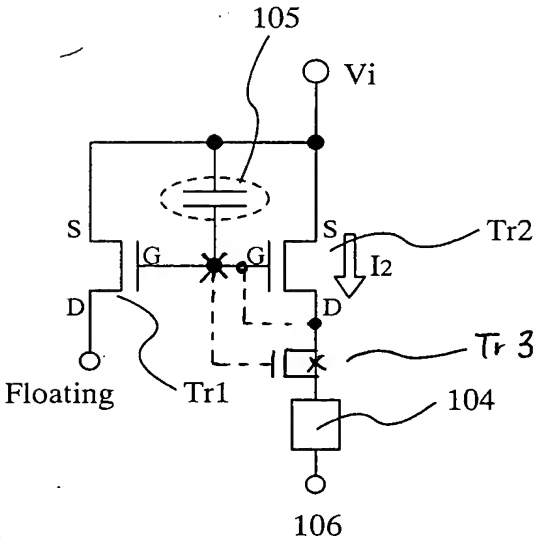

Fig. 4B

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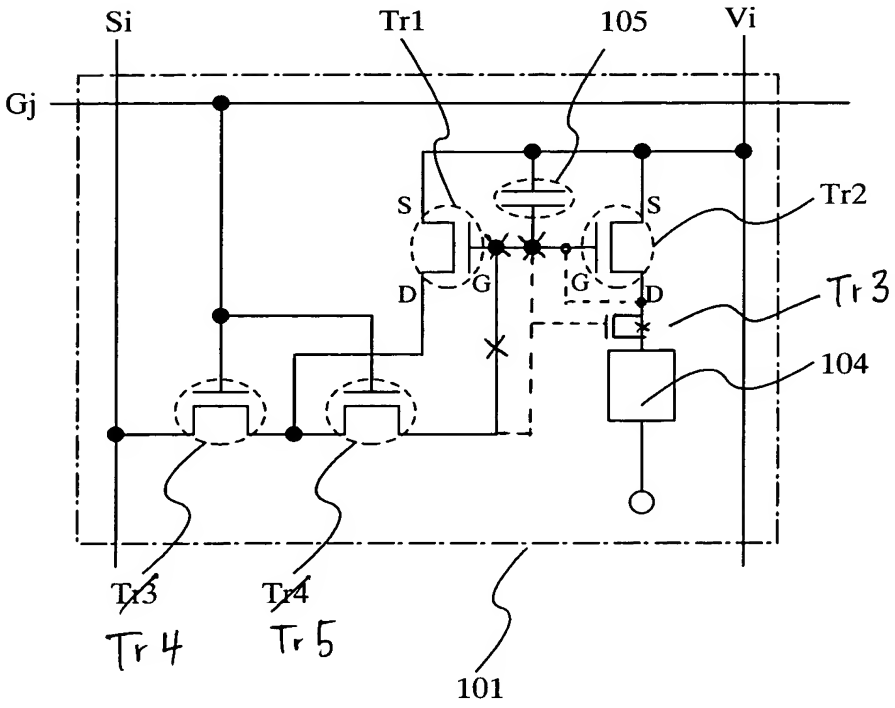

Fig. 7

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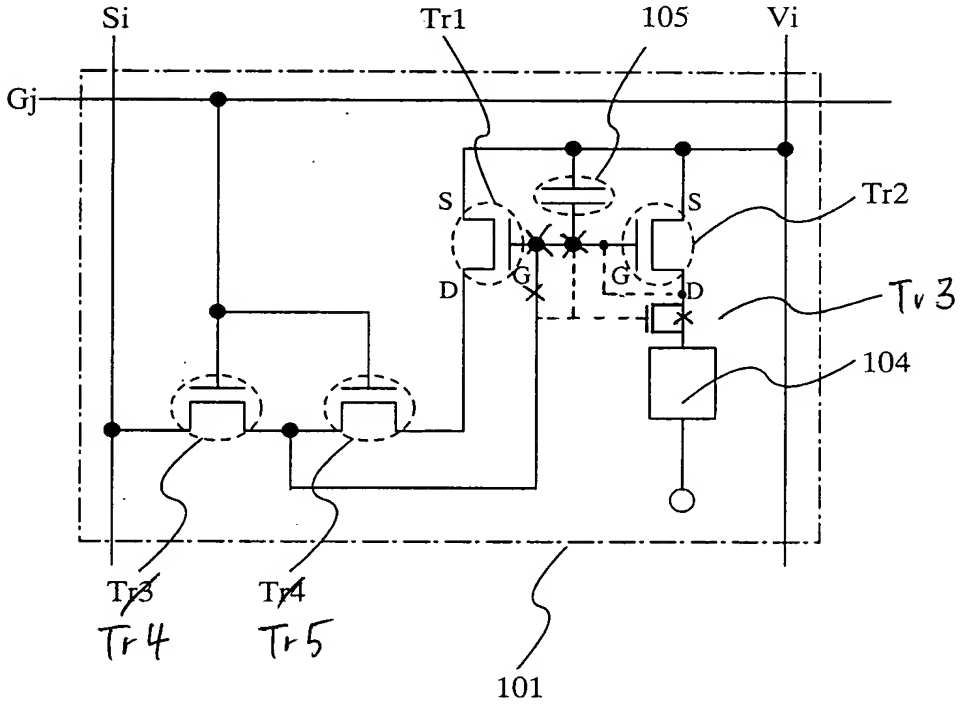

Fig. 8

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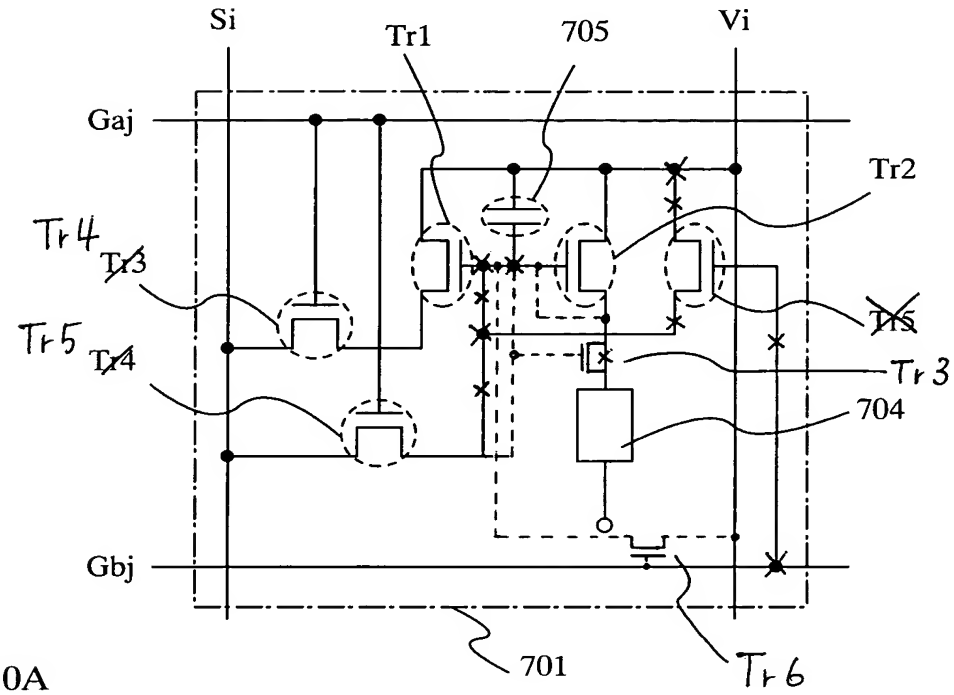

Fig. 30A

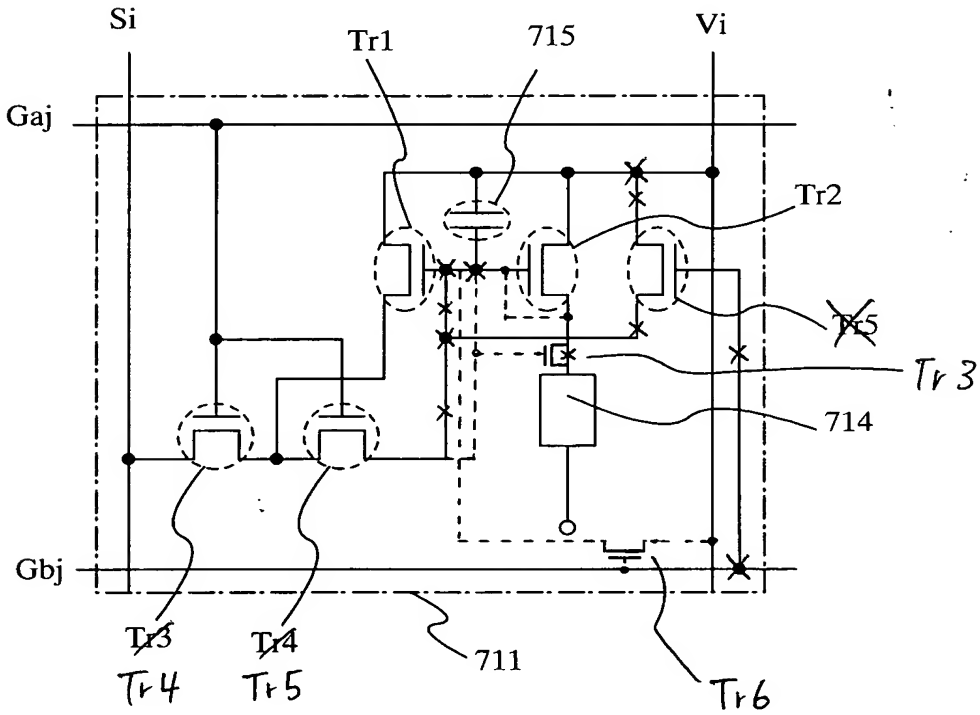

Fig. 30B

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Annotated Sheet Showing Change(s)

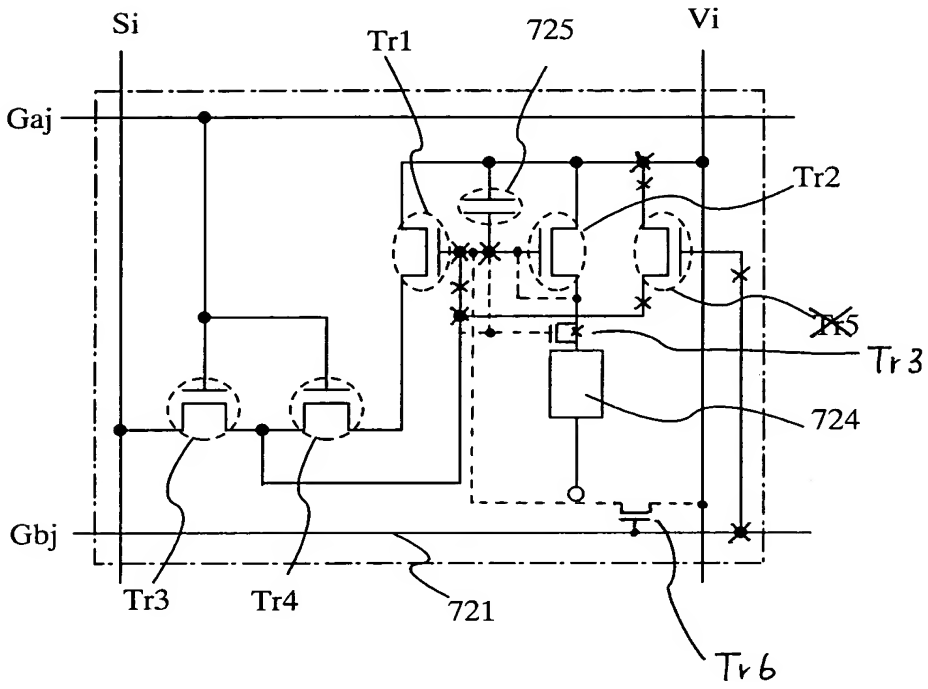

Fig. 30C

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